SHERWOOD DATA
SYSTEMS LTD

# ARCHER OWNERS MANUAL

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# 1. INTRODUCTION

## 1.1 What is Archer

Archer is a, completely self contained, single board computer (SBC). However it differs from most existing SBC'c in several important respects.

Firstly it is truly an SBC, everything is on-board, right down to the power supply and serial interface connectors. You have only to connect a mains supply to make Archer fully operational.

Secondly, complete expansion capability is built in, with an expansion bus connector containing not only the processor address, data and control lines but also logic power (5volts), auxiliary power (+/- 12volts), backup supply (3.6volts), control lines to support paged or phantom memory schemes (RAM or ROM), Direct Memory Access (DMA) and an extension of the daisy-chained interrupt scheme used by Z80 peripheral I/O chips.

Thirdly, we have provided convenient mounting holes for two expansion boards. These are used by the SDS expansion boards, and can also be used by your own custom application boards.

Fourth, a very neat and attractive case is available, either complete with mains components from SDS, or for the more cost conscious, as a kit direct from the manufacturers.

Fifth, the Archer contains a built-in watchdog circuit, often vital in professional applications, but strangely missing from most 'industrial' control boards. To go with the watchdog is a early warning power-fail circuit and the built-in capability to back-up as many as three memory sockets. That's up to 24Kbytes of non-volatile backup RAM, in addition to 16Kbytes of program ROM, all without using any memory expansion cards.

Sixth, and probably most important of all, Archer was designed by people with problems to solve, it represents their solution to a large number of everyday situations, and is now available to help you solve your problems.

## 1.2 Improvements to Archer Issue 2

The following is a list of the main areas of improvement on the revised Archer. Other than these changes there are no functional differences from issue 1. In addition to this list the body of the manual has also been revised to cover the changes.

1. The RS232C interfaces associated with J1 and J2 have been completely revised to include a more complete set of signals, and to comply better with the current common signal usage for data flow control (DTR control). These changes are detailed in a revised and expanded section 4.2.3.

2. An LED power indicator has been added to the board adjacent to J2 in such a way that on the cased versions it protrudes through the front panel. The LED is also fitted as a pcb component to uncased versions.

3. A new two pin connector, J8, has been added which can be taken to an external normally open 'RESET' switch. This switch, when closed, generates an unconditional processor /RESET signal.

4. An optional wait state generator has been added to allow the use of slower program memories, when included this increases the access time on instruction fetches (M1 cycles) to approx 350nS.

5. A new connector, J7, has been added to allow the board to be powered from an external supply. This connector, which is located underneath the mains transformer, can be fitted as an alternative to the mains power supply.

6. Space has been provisioned for a second optional 8-way DIP switch, adjacent to Sw1, which has also moved slightly. Also the order of the switch elements has been reversed so that the switch element corresponding to bit 0 is on the right hand side.

7. The processor signals /HALT and /RFSH and the battery supply have been added to the bus expansion connector J4.

8. Transient suppressor/filter components have been fitted to the mains inlet.

9. It has been made considerably simpler to adapt the board for 110V operation by provision of a suitable number of holes and the elimination of the 'Tracked-in' link joining the two primary windings in series on issue 1 boards.

10. A new and improved clock generator circuit has been used.

## 1.3 Finding what you want in this manual

This manual is arranged into six sections. Their general contents are as follows.

| | |
|---|---|
| Section 1 – | Introduction and general information. |
| Section 2 – | An introduction to the technical details of Archer, including a circuit diagram and description |
| Section 3 – | Memory layout and addressing including details of what the memory option links do, and how to alter them for specific configurations. |
| Section 4 – | I/O capability and configuration, with details of how to re-configure it, how to program the devices for specific applications, and details of the pinouts of the I/O connectors. |
| Section 5 – | Details of the system expansion connector pinouts for more advanced applications. |
| Section 6 – | Installation details, including mechanical layout and dimensions, and important wiring details of the mains connections. |

## 1.4 Getting Started

Before rushing ahead and connecting mains to the Archer, you should read the basic installation details in section 6. Note that a qualified electrician should complete the mains wiring and ensure that correct grounding precautions are observed.

If you have bought your Archer complete with the SDS Archer case, then all that is needed is to plug in your application ROM and RAM, connect the IEC mains lead supplied and go.

If your Archer has J7 fitted, rather than the mains power supply, then you should ensure the current capability of your power supply is adequate and that all connections are correct before powering up.

# 2. CIRCUIT DESCRIPTION

This section contains a general description of Archer's circuit and its operation. To illustrate many of the points covered, reference is made to the accompanying circuit diagram, at the back of this manual, which may also be found useful for reference in later sections.

The circuit coveniently splits into seven blocks. These are Processor and Memory; Parallel I/O; Serial I/O; Ramlock and Reset; Power-up and Power-fail; Watchdog; and Power Supply.

## 2.1 Processor and Memory

Archer is based around the familiar Z80A processor. It is used in a straightforward manner and run at the maximum clock speed of 4MHz. The clock oscillator circuit, IC13a/b/c/d is a simple two gate oscillator with a further two stage drive buffer.

The on-board memory is implemented through four device sockets, IC2,3,4 and 5, each of which can be configured for various RAM (Random Access Memory) or ROM (Read Only Memory) devices. The configuration of the sockets is set by altering the signals on pins 23, 26 and 28 with option links Lk1-14 detailed in sections 3.2-4 and Appendix A.

An optional 74LS74, IC19, can be used to generate a wait state on all instruction fetches, indicated by the presence of /M1. When this device is installed, the available memory access time is extended by one clock cycle, ie. by 125nS at 4MHz. This ensures that the access time for program and data fetch cycles is roughly the same.

Memory address decoding is performed by IC10a/12a/13d and is modified by Lk18 selecting which address lines are decoded to generate the four device selects. A detailed description of the settings of this link can be found in section 3.3. The address decoding circuit is enabled by /MREQ, to ensure no clash exists between memory and I/O; by RAMLOCK, which ensures no memory access can take place during power-up and power-fail; and by /CEX which allows off-board circuitry to disable the on-board memory. By controling /CEX, external circuitry can provide paged memory, overlapping the on-board address space, to extend the system capability.

I/O address decoding is performed by IC10b/11a, in a similar manner to the memory decoding. However the I/O devices themselves qualify the address as I/O through /IORQ. The address range used for the on-board I/O is F0-FF, and is summarised in Appendix A. Note that Archer expansion board products use high I/O addresses (ie. starting at hexadecimal EF and working down).

## 2.2 Parallel I/O

Parallel input/output is provided by IC8/9, a pair of Z80A-PIO devices, giving a total of 32 lines plus handshaking. These lines are taken out to two connectors, J5 and J6, which are described in detail in section 4.3. All digital port lines are terminated with a pull up resistor to simplify their use as inputs. Also, links Lk19-22 have been included to simplify the handshaking requirements, see section 4.3. Finally 8 way option switches Sw1/2 can be fitted to the ports of PIO-2 (IC7) for end user option selection etc.

## 2.3 Serial I/O

The Serial I/O circuit comprises IC6/9/14/15/20/21, a Z80A-CTC, Z80A-DART and four RS232C buffers. The CTC is used to generate the baud rate clocks for the DART as well as providing a timed interrupt facility, as described in sections 4.1 and 4.2. In addition to the normal RS232C signals, +/- 12V power and the outgoing data baud clock (RxD) are brought out on the serial 'D' connectors. Also the full complement of serial signals available is brought out to J3. For synchronous applications, the DART can be replaced with a Z80A-SIO/0, which is plug compatible with the DART. This device supports advanced synchronous bit and byte protocols such as IBM Bisync, SDLC, HDLC and CCITT-X25. It provides CRC generation and checking, sync character and zero bit insertion/deletion, flag insertion etc.

## 2.4 Ramlock and Reset circuit

The RAMLOCK and /RESET drivers IC16a/b lock out memory access and generate a system reset when a logic low input is received. Conversely they enable operation with a logic high input. These drivers have been implemented with low voltage TTL compatible op-amps to ensure the RAMLOCK and /RESET signals are correctly asserted before the processor becomes active.

## 2.5 Power-up and Power-fail

Power-up and Power-fail detection is performed by the comparator circuit based around IC16c. This circuit compares a potted down 'Raw DC' from the rectifiers with a reference voltage set by Rv1. Hence the comparator is effectively comparing the voltage across the regulator IC17 against a minimum limit set by Rv1.

At switch-on, when this voltage rises above the preset limit the comparator output changes and goes high. This signal is then delayed by R20/C7 and taken to the reset circuits to enable normal operation. The delay ensures that the clock oscillator and other circuits stabilise before /RESET is removed.
.pa
On switch-off, the comparator input voltage falls below the preset limit, causing the comparator output to go low. This signal is delayed approximately 6mS by R20,19/C7 and taken to the reset circuit to shut down normal operation before the +5v logic supply collapses. The comparator output can also be optionally taken via Lk17 and D7 to the processor /NMI ( Non Maskable Interrupt ). This allows 6mS between /NMI and /RESET for the software to perform a tidy power-down routine, see section 4.4.

## 2.6 Watchdog

The watchdog circuit comprises IC12b, IC16d, Tr1 and their associated components. IC16c, R13,14,15,16 and C6 form a low frequency oscillator whose output is connected to the ramlock and reset circuit. During normal operation the voltage on C6, which is taken to the inverting input of IC16c is lower than the reference set on the non-inverting input by R13,16, and so the output is high. However C6 can slowly charge up through R15 until its voltage increases sufficiently to make the output go low and trigger the ramlock and reset circuit.

To prevent this happening Tr1 can be made to discharge C6 at regular intervals by the software. To do this an I/O read to locations F0-F3 (CTC status read) will cause a 500nS high pulse to appear on IC12b output. This pulse is used to charge up C8 through D3 which then discharges through R17 to turn Tr1 ON, thus discharging C6. The time between discharges must be less than 2000mS to prevent a /RESET being generated.

## 2.7 Power Supply

The on-board mains power supply circuit has been kept as simple as possible within the needs of the board. Logic supply regulation is provided by IC17, and the logic supply has its own rectifiers, to minimise the ripple on the +/-12v rails. By mounting the transformer on the pcb the whole unit is kept extremely compact and neat, and avoids the problem of having to mount the power supply separately.

Note that the +/-12v rails are not regulated, as they adequately meet the RS232C requirements. However regulators may be required if sensitive analogue circuits are to be added on an off-board expansion card.

The maximum loading of the supplies by expansion cards is a total of 400mA from the +/-12V and 5V rails, see table 2.1 below.

If Archer is to be built into a system which already has its own power supplies, or if the off-board requirements exceed those available, then the mains power supply may optionally be omitted altogether and replaced by a power connector, J7, to accept external power input, see Section 5.

| Supply | Max off-board load | |
|---|---|---|
| | (1) or | (2) |
| + 5v | 200mA | 100mA |
| +12v | 0mA | 50mA |
| -12v | 0mA | 50mA |

TABLE 2.1 Off-board supply loading

## 3. MEMORY

Archer has four memory sockets suitable for either ROM or RAM devices in the popular 24 pin or 28 pin packages. To allow for a wide range of device types and uses, there are a number of configuration links on the Archer. When shipped, Archer is set to the most popular configuration as follows-

| Socket | Addr | Device types |
|---|---|---|
| IC 2 | 0000h | PROM type 2732/A or 2764 |
| IC 3 | 2000h | RAM type 2016 or equiv (no backup) |
| IC 4 | 4000h | RAM - - - - - - |
| IC 5 | 6000h | RAM - - - - - - |

TABLE 3.1 Factory set memory configuration

For more details on option settings see tables 3.2 and 3.3 below.

### 3.1 Memory types

All four memory sockets on the Archer are identical, except that socket IC2 cannot support a backup RAM. This is not significant as it will normally contain a program PROM since the reset start address for the Z80 processor is 0000h, which is always the base address for socket IC2.

### 3.2 Device types supported

Table 3.2 below gives a matrix of the device types supported by Archer. Note that this table is far from complete as many manufacturers have their own product numbering schemes, particularly for the RAM's. Section 3.4 deals with how to select the link positions for devices other than the ones shown.

| Description | | Socket | link numbers | | |
|---|---|---|---|---|---|
| type number | layout | IC2-<br>IC3-<br>IC4-<br>IC5- | Lk1<br>Lk2<br>Lk3<br>Lk4 | Lk5<br>Lk8<br>Lk11<br>Lk14 | --<br>Lk7<br>Lk10<br>Lk13 |
| 2716 | 2Kb ROM | | 2 | 3 | 1 |
| 2732/A | 4Kb ROM | | 2 | 2 | 1 |
| 2764 | 8Kb ROM | | * | 2 | 1 |
| 27128 | 16Kb ROM | | 1 | 2 | 1 |
| 2016 | 2Kb RAM | | 2 | 1 | 1 |
| 6116 | 2Kb RAM | | 2 | 1 | 1/2 |
| 5564 | 8Kb RAM | | 2 | 2 | 1/2 |

TABLE 3.2 Memory device selection - option links Lk1-14

notes:

1. Lk7,10,13 position 2 selects backup supply for suitable RAM's
2. EPROMS (27---) must be Intel style single rail devices
3. * means don't care ( 1,2 or no connect )
4. Program memory should have an access time of 250nS or less (350nS or less if IC19 is fitted)
5. Data memory should have an access time of 350nS or less

## 3.3 Memory address decoding

It would have been possible to decode the memory sockets to fixed addresses, regardless of the memory devices to be used, so, for example, 2Kb devices would always have to fit into a 16Kb slot. This is clearly very wasteful of address space, particularly when we want expansibility. Some form of address decoding is clearly desirable. The dual link Lk18 performs this function, allowing the four memory slots to be decoded as shown in Table 3.3.

| Lk18 | size | IC-2 | IC-3 | IC-4 | IC-5 |
|---|---|---|---|---|---|
| 1-2 + 3-4 | 2Kb | 0000-07FF | 0800-0FFF | 1000-17FF | 1800-1FFF |
| 2-3 + 4-5 | 4Kb | 0000-0FFF | 1000-1FFF | 2000-2FFF | 3000-3FFF |
| 5-6 + 7-8 | 8Kb | 0000-1FFF | 2000-3FFF | 4000-5FFF | 6000-7FFF |
| 6-7 + 8-9 | 16Kb | 0000-3FFF | 4000-7FFF | 8000-BFFF | C000-FFFF |

TABLE 3.3 Memory address decoding selection - Lk18

notes:

1. If a small size memory device is in a large capacity slot it 'mirrors' itself throughout the memory slot eg. A 2Kb RAM in an 8Kb slot would appear reflected four times at 0 to 2, 2 to 4, 4 to 6 and 6 to 8Kb. Any of these reflections is valid and could be used, for example, to make two 2Kb RAM's in consecutive 8Kb slots appear as contiguous memory.

2. As the address decoding is generally not complete, ie. some address lines are not decoded, There will be reflections of the decoded memory slots throughout the address space. In the first case in Table 3.3 for example, memory is only fully decoded from 0000 to 1FFF; this decode map will mirror itself a total of eight times throughout the processor address space. ie at 2000-3FFF, 4000-5FFF etc. This 'unused' memory space is not lost though, it can be recovered by expansion cards using a control line on the bus expansion header. It is possible, in fact, to completely overide the on-board address decoders. This will be dealt with in section 5, for now Table 3.3 applies.

## 3.4 Selecting other memory devices

To fit a memory device not listed in Table 3.2 the configuration links need to be set suitably. The memory socket signal configuration is shown below in Table 3.4. From this, check that all the signals required are in the correct positions and set up the option links accordingly.

As a general rule devices pined out to the JEDEC standard with /OE on pin 22 and /CE on pin 20 (pins 20 and 18 on a 24pin device) are suitable, although some devices with dual /CE conections may also be suitable. The access time from /CE or /OE to data valid should be less than 250nS for program memory (350nS if IC19 is fitted) or 350nS for data memory, using the standard 4MHz clock.

```
                                                     |  Selection Links
                                                     |-------------------
               ______ ______                         |
 VCC    1   |        U        |  28  VCC-BAT ---------   *   7   10   13
 A12    2   |    ___ ___      |  27  /WR             |
  A7    3   | |1  U  24|      |  26  VCC-BAT-A13 -----   1   2    3    4
  A6    4   | |        |      |  25  A8              |
  A5    5   | |        |      |  24  A9              |
  A4    6   | |        |      |  23  /WR-A11-VCC -----   5   8   11   14
  A3    7   | |        |      |  22  /RD             |___________________
  A2    8   | |        |      |  21  A10             |  IC2 IC3 IC4 IC5
  A1    9   | |        |      |  20  /CE             |___________________
  A0   10   | |        |      |  19  D7
  D0   11   | |        |      |  18  D6                   * no link
  D1   12   | |        |      |  17  D5
  D2   13   | |        |      |  16  D4               Note position
 GND   14   |_|________|_|    |  15  D3              of 24pin device
```

TABLE 3.4 Memory Socket Device Connections

## 3.5 Debuging Memory Problems

If, after installing memory in the sockets, it does not appear to be operating correctly, the following check list should be followed to ensure correct installation.

1. Are the memory devices in the correct sockets? IC2 is low memory address, IC5 is high memory address, see Table 3.3.
2. Are all the pins of the memory devices correctly inserted and not outside the socket or folded underneath?
3. Is the memory address decoding link Lk18 set correctly for the memory devices installed? See Table 3.3.
4. Are any 24 pin memory devices installed incorrectly in their sockets? Pin 1 of a 24 pin device should be in pin 3 of the socket, see Table 3.4 and diagram.
5. Are the option links Lk1 to 14 set correctly for the memory devices installed? See Tables 3.2 and 3.4. In particular check links Lk7,10 and 13 are correct for all devices.
6. Are battery backed RAM's suitable to be battery powered? They should be CMOS or eqivalent devices, not normal NMOS.
7. Are the memory devices fast enough? Program memory should have an access time of 250nS or less (350nS or less with IC19 fitted), data memory should be 350nS or less.
8. Is the software using the same physical memory more than once, perhaps by making wrong assumptions about the 'mirroring' effect caused by incomplete address decoding? This can often fool crude memory sizing routines. See Table 3.3 and notes. If you have the SDS Monitor then it is a good idea to check out all memory using the memory test facility (^T command).
9. If a memory expansion board is fitted, is it disabling the on-board memory? See section 5 or remove the expansion memory to check.
10. Is the watchdog circuit coming into operation, thus disabling the on-board memory? Remove the watchdog enable link Lk16 to check, see section 4.4.3.
11. Is the power-fail circuit coming into operation, causing a non maskable interrupt and then ramlock and reset. This could be due to Rv1 being incorrectly set. Remove the power-fail enable link Lk17 to check, and see section 4.4.1 on how to adjust Rv1.

# 4. INPUT OUTPUT

Archer is essentially a control engine, rather than a pure computing engine. Its capability is therefore largely measured by its ability to do input/output.

There are six input/output subsystems which need to be considered separately. These are-

1. The Counter Timer Circuits
2. The Serial input/outputs
3. The Parallel input/outputs
4. The Watchdog/Reset circuit
5. The Bus expansion header
6. The Serial expansion header

As might be expected, these subsystems interact to support one another, and this will be illustrated as we go along.

## 4.1 The Counter Timer Circuits

The Counter Timer Circuit chip (CTC) provides four independent, programmable channels for system timing, which can be programmed to act in either a counter or a timer mode. In Archer the counter input is connected to the processor clock divided by two (fc/2), as this increases the available timer range.

There are two main uses for the CTC channels. Firstly they can be used as baud rate clocks for the serial input/output channels. CTC-0 is reserved to generate both the receive and transmit baud rate clocks for DART-B (RxTxC), and CTC-2 is reserved to generate the transmit baud rate clock for DART-A (TxC). The receive baud rate clock for DART-A (RxC), can be derived from either the same source as the transmit clock, CTC-2, or from CTC-1, or obtained from the serial header J3, depending on the position of Lk23.

<table>
<tr><th rowspan="2">DART clock</th><th colspan="3">clock source</th></tr>
<tr><th>Lk23-1</th><th>Lk23-2</th><th>open</th></tr>
<tr><td>RxTxC-B</td><td colspan="3">-------- CTC-0 --------</td></tr>
<tr><td>TxC-A</td><td colspan="3">-------- CTC-2 --------</td></tr>
<tr><td>RxC-A</td><td>CTC-1</td><td>CTC-2</td><td>J3/13</td></tr>
</table>

TABLE 4.1 Baud Clock selection

Secondly the CTC's can be used to generate a timed interrupt to the processor, to perform some time critical function eg. maintain a time of day clock. Even if CTC-0,1 and 2 are used for baud rate generation, CTC-3 is free for this purpose.

### 4.1.1 CTC Programming

The four CTC channels CTC-0 to 3 are at hexadecimal addresses F0-F3 respectively. All four CTC channels are programmed identically. The format of the control word sent to the channel control register is shown below.

| Intr | Mode | Rnge | Slop | Trig | Time | Res | Func |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| Intr | Interrupts enabled if true (1) |
| Mode | Sets timer mode (0) or counter mode (1) |
| Rnge | Timer prescale of 16 (0) or 256 (1) |
| Slop | ----------------- not applicable ----------------- |
| Trig | Start on time const load (1) or continuous (0) |
| Time | Time const byte follows (1) or not (0) |
| Res | Software reset if true (1) |
| Func * | Identifies control byte (1) or vector (0) below |

* The interrupt vector can only be set when addressing CTC-0. When loaded, D7-D3 are stored for use during an interrupt cycle. If the CTC has one or more interrupts enabled, it can supply Interrupt Mode 2 vectors to the Z80A CPU. These vectors are made up from V3-V7 supplied by the user, with V1-V2 inserted by the CTC depending on the channel, and V0=0, ensuring the vector address is on a word boundary.

The CTC timer values can also be read whilst timing. However this is most useful when the CTC channels are being used as counters, and they are effectively only timers here. Data reads to I/O addresses F0-F3 are therefore reserved for use with the watchdog circuit which uses the same addresses.

For further details on programming the CTC please refer to the full Z80A-CTC data sheets.

## 4.2 Serial Input Output

The serial input/output is provided by a Dual Asynchronous Receiver/Transmitter chip (DART). This provides two independent programmable serial communication channels, and is identical in every way to the better known SIO/0 in asyncronous mode. For syncronous applications the SIO/0 can directly replace the DART.

The DART is addressed at hexadecimal locations F4-F7 as below

| | DART-A | DART-B |
|---|---|---|
| Data port address | F4 | F5 |
| Control port address | F6 | F7 |
| TxC - Tx baud clock | CTC-2 | CTC-0 |
| RxC - Rx baud clock | * CTC-1/2 | CTC-0 |
| Data Connector | J1 | J2 |

TABLE 4.2 Serial Channel Particulars

* Depending on Lk23, see Table 4.1

### 4.2.1 DART write registers

The DART contains six registers (WR0-5) in each channel that require programming separately by the user. With the exception of WR0, programming the write registers requires two bytes. The first byte is written to WR0 and contains three bits that point to the required register (R2-R0 below). The second byte is the actual control data that is written to the selected register. WR0 is a special case that can be written to directly and allows all the basic commands to be accessed with a single byte.

WR0 Register pointers, mode initialisations etc

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| not – | used | C2 – | C1 – | C0 | R2 – | R1 – | R0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| C2 | C1 | C0 | |
|---|---|---|---|
| 0 | 0 | 0 | null code |
| 0 | 0 | 1 | not used |
| 0 | 1 | 0 | reset ext/status interrupts |
| 0 | 1 | 1 | channel reset (see note below) |
| 1 | 0 | 0 | enable Int on next Rx character |
| 1 | 0 | 1 | reset TxInt pending |
| 1 | 1 | 0 | error reset |
| 1 | 1 | 1 | return from Int (channel A only) |

R2-R0 Register select in the range 0-5 (000-101 binary)

## WR1 Interrupts and Data transfer definitions

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Wait/Ready status | | | | | Vect | | |
| Ena | Func | RxTx | RxI1 – | RxI0 | Stat | TxI | ExtI |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | | |
|---|---|---|
| Ena | Enable Wait or Ready function | > not used on |
| Func | Define as Wait or Ready | > unexpanded |
| RxTx | Wait or Ready on Rx/Tx | > card |

| RxI1 | RxI0 | |
|---|---|---|
| 0 | 0 | Rx Interrupt disable |
| 0 | 1 | Rx Interrupt on first character |
| 1 | 0 | Rx Interrupt on all chars, Parity effects vector |
| 1 | 1 | Rx Interrupt on all chars, Parity has no effect |

| | |
|---|---|
| Vect Stat | Status effects vector if true (1) |
| TxI | Enable Transmit Interrupts if true (1) |
| ExtI | Enable External Interrupts if true (1) |

## WR2 Interrupt Vector ( channel B only )

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| V7 – | V6 – | V5 – | V4 – | V3 – | V2 – | V1 – | V0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| V7–V0 | Interrupt Vector base address (V0 must be 0) |

## WR3 Receive Parameters and control

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Data Length | | Auto | | | | | Rx |
| L1 – | L0 | En | ------- | not | used | ------- | Ena |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| L1 | L0 | |
|---|---|---|
| 0 | 0 | Rx 5 bits/character |
| 0 | 1 | Rx 7 bits/character |
| 1 | 0 | Rx 6 bits/character |
| 1 | 1 | Rx 8 bits/character |

| | |
|---|---|
| Auto En | Auto Enables if true (1) |
| Rx Ena | Enable Receiver if true (1) |

WR4 Tx, Rx miscellaneous parameters and modes

| X1 | - X0 | not | - used | S1 | - S1 | Par E/O | Par En |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| X1 | X0 | |
|---|---|---|
| 0 | 0 | x1 clock mode |
| 0 | 1 | x16 clock mode |
| 1 | 0 | x32 clock mode |
| 1 | 1 | x64 clock mode |

| S1 | S0 | |
|---|---|---|
| 0 | 0 | not used |
| 0 | 1 | 1 stop bit |
| 1 | 0 | 1.5 stop bits |
| 1 | 1 | 2 stop bits |

| | |
|---|---|
| Par E/O | Parity Even (1) or Odd (0) |
| Par En | Parity Enable if true (1) |

WR5 Transmit Parameters and controls

| DTR | L1 | - L0 | Brk | TxEn | not used | RTS | not used |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| L1 | L0 | |
|---|---|---|
| 0 | 0 | Tx 5 Bits/character |
| 0 | 1 | Tx 7 Bits/character |
| 1 | 0 | Tx 6 Bits/character |
| 1 | 1 | Tx 8 Bits/character |

| | |
|---|---|
| DTR | Data Terminal Ready output bit |
| Brk | Transmit Break |
| TxEn | Transmit Enable |
| RTS | Request To Send output bit |

### 4.2.2 DART Read registers

The DART contains three registers (RR0-RR2) that can be read to obtain status information for each channel. (except RR2 which applies to channel B only). The status information includes error conditions, interrupt vectors and the standard communications interface signals. To read the contents of a selected register other than RR0, the user must first write a pointer byte to WR0 in exactly the same manner as a write register operation. Then, by executing an input instruction, the contents of the addressed register can be input to the CPU.

### RR0 Transmit / Receive status

| Brk | not used | CTS | RI | DCD | Tx Clr | Int Pend | Rx char |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| Brk | Break state detected |
| CTS | CTS input true |
| RI | Ring Indicator input true |
| DCD | Data Carrier Detect input true |
| TxClr | Transmit buffer empty |
| IntPend | Interrupt pending (channel A only) |
| RxChar | Receive character available |

### RR1 Special receive condition status

| not used | FE | ORun | PE | --- not used --- | | | Sent |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| FE | Framing error found |
| ORun | Over-Run error found |
| PE | Parity error found |
| Sent | All Sent |

### RR2 Modified Interrupt Vector ( channel B only )

| V7 | V6 | V5 | V4 | V3 | V2 | V1 | V0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| V7-V4 | Basic interrupt vector |
| V3-V1 | Modified vector if 'status affect vector' |
| V0 | must be '0' |

If the DART has one or more interrupts enabled, it can supply Interrupt Mode 2 vectors to the Z80A CPU. These vectors are made up from V7-V0 supplied by the user, with V3-V1 modified by the DART depending on the channel and status; V0 must 0, to ensure the interrupt vector address is on a word boundary.

For further details on programming the DART or SIO/0 please refer to the full Z80A-DART/SIO data sheets.

### 4.2.3 Serial Data Connectors

Archer contains two standard female D-type 25 way serial data connectors. These are wired in accordance with the standard for Data Communication Equipment (DCE), as normally found on communication equipment. The pin definitions are shown below.

| Pin | RS232C Name | DART Name | Dir. | Signal description |
|---|---|---|---|---|
| 1 | FG | Earth | - | Protective ground |
| 2 | TxD | RxD | in | Terminal Data |
| 3 | RxD | TxD | out | Comms Data |
| 4 | RTS | DCD | in | Request To Send |
| 5 | CTS | DTR | out | Clear To Send |
| 6 | DSR | RTS | out | Data Set Ready |
| 7 | SG | - | - | Signal ground/return |
| 8 | RLSD | RTS | out | Rx Line Signal Detected |
| 9 | - | - | out | +12v = RS232C 'TRUE' |
| 10 | - | - | out | -12v = RS232C 'FALSE' |
| 14 | STD | RI | in | General purpose input |
| 17 | RSET | TxC | out | Rx Signal Element Timing |
| 20 | DTR | CTS | in | Data Terminal Ready |

TABLE 4.3 Serial Data Connectors J1 and J2

Note that the RS232C pin marked TxD (Transmitted Data) is actually an input and similarly RxD is actually an output. This is because RS232C defines inputs and outputs in terms of the Data Terminal Equipment (DTE), not the Data Communication Equipment (DCE). It is important to understand this difference as pins on the DART are named by the manufacturer in accordance with the DTE standard, hence the input marked Rx on the DART is connected to the input marked TxD in the table above.

Similarly the input marked CTS on the DART, and in the status register RR0 described above, is actually connected to the RS232C pin labeled DTR and the same principle, in reverse, also applies to the DTR output on the DART which goes to the pin labeled CTS.

When programing the DART it is also important to realise the special functions provided by various inputs and outputs (see Table 4.4 below). The CTS input mentioned above, for instance, can be used to automatically disable the transmitter when false (-12volts). This makes CTS ideal for data flow control, which by convention (not specification) arrives on the DTR input.

For this reason we recommend the use of pins 5 and 20 for flow (start/stop) control and pins 4 and 8 for link control. A cable to link together two Archers would therefore cross signal lines 2 and 3 (data); 5 and 20 (flow control); 4 and 8 (link control) and directly connect pins 1 and 7 (Grounds).

| Pin | RS232C Name | DART Name | Special Function |
|---|---|---|---|
| 4 | RTS | DCD | Enables Rx if 'true' in auto mode |
| 5 | CTS | DTR | none |
| 6 | DSR | RTS | Delays 'false' until Tx empty |
| 8 | RLSD | RTS | - - - - - |
| 14 | STD | RI | Interrupt Z80A on both transitions |
| 20 | DTR | CTS | Enables Tx if 'true' in auto mode |

TABLE 4.4 Special Functions of Serial Signals

In addition to the normal D-type 25 way connectors, a full range of serial communication signals is made available on a 26 way IDC type header J3. This would be used primarily with synchronous communications hardware in conjunction with an SIO/0 replacing the DART. Connection details for J3 can be found in section 5.

### 4.2.4 Programming example 1

The following program segment shows a typical example of setting up a serial channel for communication at 9600 baud. Serial channel A is used, with link 23 set in position 2 (Receive baud clock same as transmit baud clock, see table 4.1 or Appendix A).

```
ctcch2     equ       0F2H
siocha     equ       0F4H

; First set up the CTC for counter mode, divide by 13
; to give 4000/(2*13) = 153.8kHz = 9600*16Hz
START:     ld        a,47H
           out       (ctcch2),a     ; mode
           ld        a,13
           out       (ctcch2),a     ; count

; Now set up the DART, this is done with a block move
; instruction outputting a table of values
           ld        c,siocha+2     ; channel A control
           ld        hl,table       ; table start addr
           ld        b,tablen       ; table length
           otir                     ; output bytes
           ret

TABLE:     db        18H            ; reset channel
           db        04H,4CH        ; WR4- x16, no parity
           db        05H,68H        ; WR5- Tx enable, 8 bits
           db        03H,C1H        ; WR3- Rx enable, 8 bits
           db        01H,00H        ; WR1- no interupts
tablen     equ       $-table        ; length of table
```

## Programming example 2

Continuing from example 1 above, three subroutines are given below for console status (CONST), console input (CONIN) and console output (CONOUT).

```
; Console status routine checks if a character has been
; received and sets the Z flag accordingly (1 = no char)
CONST:     in        a,(siocha+2) ; read status register
           bit       0,a
           ret

; Console input routine waits until a character has been
; received and then returns it in register A.
CONIN:     call      const
           jr        z,conin        ; wait for character
           in        a,(siocha)     ; then get it
           res       7,a            ; clear top bit
           ret

; Console output routine waits until the transmitter is
; available and then sends the character in register A.
CONOUT:    push      af             ; save character
CONO1:     in        a,(siocha+2)
           bit       2,a
           jr        z,cono1        ; wait for transmitter
           pop       af
           out       (siocha),a     ; send character
           ret
```

## Programming example 3

The following subroutine is used to set the baud rates of the serial channel above to one of a number of values. A code is sent to the subroutine in register A to select the desired rate.

```
; First convert the baud rate code in register A into a
; table entry address.
BAUDSET:  and       7H           ; restrict range to 0-7
          rlca                   ; two bytes per entry
          ld        hl,baudtab   ; add table base address
          add       a,l
          ld        l,a
          ld        a,h
          adc       a,0
          ld        h,a          ; hl points to table entry
          ld        c,ctcch2     ; CTC port address
          outi                   ; output two entries
          outi
          ret

BAUDTAB:  db        47H,13       ; 9600 baud - 0
          db        47H,26       ; 4800 baud - 1
          db        47H,52       ; 2400 baud - 2
          db        47H,104      ; 1200 baud - 3
          db        07H,26       ;  600 baud - 4
          db        07H,52       ;  300 baud - 5
          db        07H,142      ;  110 baud - 6
          db        27H,20       ;   50 baud - 7
```

Note: The above examples assume a system clock of 4.0000MHz, which does not conveniently divide down to give a baud rate of 19200 or 38400. Both of these baud rates can be obtained by changing the system clock frequency to 3.6864MHz, at the expence of a slight loss of processor speed (approx 8.5%). The contents of BAUDTAB would also reqire revising accordingly.

## 4.3 Parallel Input output

The parallel input output (PIO) capability of Archer comes from two Z80A-PIO chips, each of which offer two independent 8-bit bidirectional programmable parallel ports with handshaking. These can be programmed for byte input, byte output, byte input/output (port A of each device only), and bit input/output. The PIO chips are fully compatible with the Z80A vectored interrupt scheme and can interrupt on peripheral data input patterns. eg. keyboard data ready. Port B of each PIO is also capable of directly driving darlington power output transistors.

PIO-2 additionally has the facility to have DIL switches fitted to one or both of its ports. These are mounted close to the edge of the pcb so they can be accessed through the front panel of an Archer case for user option selection.

The PIO hexadecimal port addresses etc. are listed in Table 4.5

| Detail | PIO-1 | PIO-2 |
|---|---|---|
| Port A data address | F8 | FC |
| Port A control address | FA | FE |
| Port B data address | F9 | FD |
| Port B control address | FB | FF |
| | | |
| Port A /STB link ref. | Lk21 | Lk19 |
| Port B /STB link ref. | Lk22 | Lk20 |
| Signal connector | J6 | J5 |

TABLE 4.5 Parallel I/O port particulars

### 4.3.1 PIO control registers (Modes 0,1,2)

Programming a PIO port to act in Mode 0, 1, or 2 (Byte Output, Input, or Bidirectional) requires two bytes. The first byte is the Mode Control Byte.

Mode Control Byte

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| M1 | - M0 | --not | used- | 1 | - 1 | - 1 | - 1 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| M1 | M0 | |
|---|---|---|
| 0 | 0 | Mode 0 - Byte Output |
| 0 | 1 | Mode 1 - Byte Input |
| 1 | 0 | Mode 2 - Bidirectional |
| 1 | 1 | Mode 3 - Bit Input/Output |

Note that the four lower bits identify the Mode Control Byte.

The second byte is the Interrupt Vector Byte and is required only if interrupts are enabled.

Interrupt Vector Byte

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| V7 | V6 | V5 | V4 | V3 | V2 | V1 | 0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| V7-V1 | Upper seven bits of interrupt vector (V0=0) |
| D0 | Is zero to identify the vector control byte |

There is one additional control byte which may be issued at any time, that is the Interrupt Enable control.

Interrupt Enable Control byte

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Int | --- not used --- | | | 0 | 0 | 1 | 1 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| Int | Interrupts Enabled if true (1) |
| D3-D0 | Identify the Interrupt Enable Control byte |

## 4.3.2 PIO control registers (Mode 3)

To program a PIO port in Mode 3 (bit input/output) requires a Mode Control Byte, followed by three additional control bytes as below, followed by an interrupt vector control byte if interrupts are enabled, or are going to be enabled.

I/O Register Control byte

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

P7-P0 define the eight port bits as Input (1) or Output (0)

Interrupt Control byte

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Ena | Func | Levl | Mask | 0 – | 1 – | 1 – | 1 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| Ena | Interrupt Enabled if true (1) |
| Func | Mask byte function AND (1) or OR (0) |
| Levl | Active level is HIGH (1) or LOW (0) |
| Mask | Mask byte follows if true (1) |
| D3-D0 | Identify the Interrupt Control byte |

Mask Control byte (only if Mask = 1 above)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

| | |
|---|---|
| M7-M0 | Mask bits: A bit is monitored for an interrupt only if the bit is defined as input and the mask bit is set to zero (0). |

In addition, an Interrupt Enable Control byte, as described above may be issued at any time.

### 4.3.3 PIO Port connectors

Each of the two PIO's has its own I/O connector for interfacing to external circuitry. These two connectors, which have identical pin definitions, provide connections to the two eight bit port lines, four handshaking lines, and power (+5v, 0v, and +/-12v). The total power taken from these and the system expansion connectors, see section 5, must not exceed the figures given in section 2.7.

PIO port connectors J5 and J6

```
                  1     2

        +12V      +     +     -12V
         +5V      +-----+     +5V
          0V      +-----+     0V
Port A bit 6      +     +     Port A bit 7
 -  -  -   4      +     +      -  -  -   5
 -  -  -   2      +     +      -  -  -   3
 -  -  -   0      +     +      -  -  -   1
 -  -   /RDY      +     +      -  -   /STB
Port B bit 6      +     +     Port B bit 7
 -  -  -   4      +     +      -  -  -   5
 -  -  -   2      +     +      -  -  -   3
 -  -  -   0      +     +      -  -  -   1
 -  -   /STB      +     +      -  -   /RDY

                 25    26
```

### 4.3.4 PIO Port handshake selection links

When used in Modes 0,1 or 2 data transfers to and from the Ports are controlled by two handshaking lines, /STB (input) and /RDY (output). Links Lk19-22 (see Table 4.5 above) allow hardwired configurations on these lines to simplify interfacing in many cases. The effect of these links is shown in Table 4.6.

| Lk19 etc | Effect |
|---|---|
| none | Allows external circuitry to control |
| 1 | generates 250nS high pulse on output |
| 2 | generates 250nS low pulse on output |

TABLE 4.6 Effect of /STB links Lk19-22

## 4.4 Watchdog and Reset Circuits

The Watchdog and Reset circuits perform several functions which should each be considered separately. They are, in the order we will consider them.

1. Power-Fail : /NMI, RAMLOCK and /RESET generation
2. Power-up : /RESET timing
3. Watchdog : RAMLOCK and /RESET generation
4. Reset Switch : Addition of a /RESET switch

### 4.4.1 Power-Fail

Throughout normal operation the rectified and smoothed AC voltage supplying the 5V regulator is monitored by a comparator. As soon as this falls below a safe value the comparator output switches, generating /PFAIL. This signal is used in two places. First it goes, via Lk17, to the /NMI input on the processor, allowing the optional generation of a Non Maskable Interrupt on power-failure.

| Link Lk17 | Effect |
|---|---|
| In | Power-fail generates NMI |
| Out | No effect |

TABLE 4.7 Effect of Lk17 on Power-fail

Secondly /PFAIL is taken via a delay circuit to generate RAMLOCK and /RESET. The purpose of the delay is to allow time for a Non Maskable Interrupt routine to run, see the timing diagram below. After the delay period two signals, RAMLOCK and /RESET, occur together. RAMLOCK disables all on-board memory, whilst /RESET provides a system wide reset initialisation.

The switching level of the comparator is adjusted by Rv1 which is supplied suitably set for all normal use. Usually therefore this pot should not be adjusted. In some circumstances however it may be found necessary to adjust the comparator level, such as if the mains voltage is abnormally low or the supply drains have been increased by expansion boards.

If the comparator level is increased (clockwise rotation) a quicker detection of an impending power-failure is given, but at the expense of a reduced safety margin for low mains voltages, additional supply rail current drains etc.

If the comparator level is decreased, a good immunity to minor supply voltage and load fluctuations is obtained, but at the expense of a shortened period for the NMI routine to act, see the power-fail diagram below. The normal setting, as measured on TP2, is 2.0V.

### 4.4.2 Power-up

On power-up the same circuit that detects power-failure detects when the regulator input voltage has risen high enough to ensure that the 5V logic supply is present. This signal is then delayed further to ensure the circuit is fully settled before enabling the memory and deactivating the reset signal.

### 4.4.3 Watchdog Operation

The Watchdog circuit is essentially an oscillator whose output is fed, via Lk16, to the RAMLOCK and /RESET drivers.

| Link Lk16 | Effect |
|---|---|
| In | Watchdog generates /RESET |
| Out | No effect |

TABLE 4.8 Effect of Lk16 on /RESET

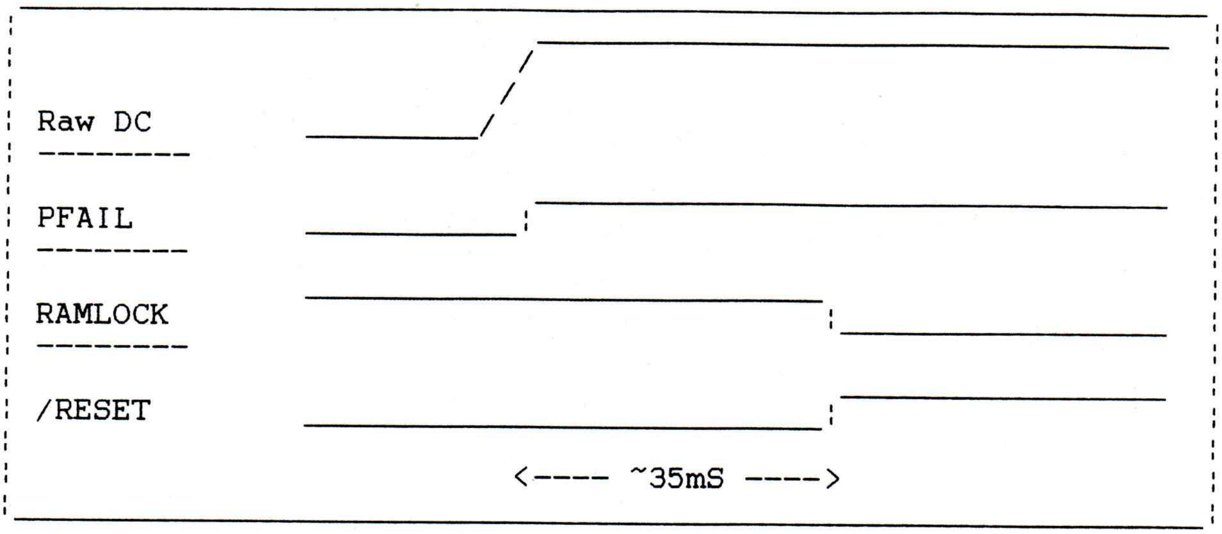
The Watchdog oscillator has two states, reset and active. In its reset state RAMLOCK and /RESET are true, and the processor and memory are disabled. In its active state the circuit allows the processor to run. The processor can keep the oscillator in its active state by doing I/O reads from hexadecimal addresses F0-F3 inclusive. The natural period of the active state is greater than 2000 mS, so to ensure the reset state never occurs read cycles must occur at least this often.

Note The watchdog hold-off addresses, F0-F3, are the same as the CTC status register read addresses. Care should therefore be taken if both features are required.

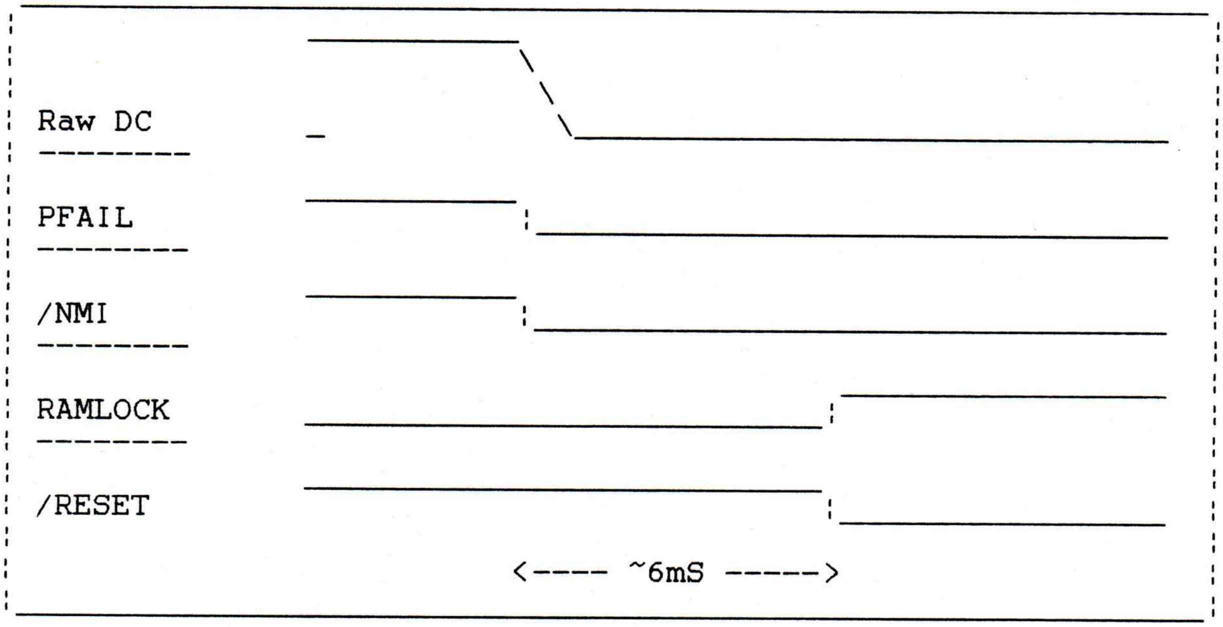
### 4.4.4 Reset Switch

The connector J8 is provided to enable an external switch to discharge the /RESET timing capacitor, hence generating an immediate processor reset. This facility can be used not only to recover from a crashed program, but also as a means of forcing a known event, such as re-reading the option switches.

Power-up signals


Raw DC
PFAIL
RAMLOCK
/RESET
<---- ~35mS ---->

Power-fail signals


Raw DC
PFAIL
/NMI
RAMLOCK
/RESET
<---- ~6mS ----->

## 5. EXPANSION CONNECTORS

To assist in system expansion, two expansion bus headers are provided. The first system expansion header brings out the full complement of serial interface signals, allowing for the use of an SIO/0 rather than the asynchronous only DART.

The second expansion header is essentially the processor bus which has been brought out to a 50 pin connector. These connectors are used by current and planned SDS expansion boards.

Both expansion connectors also bring out the supply rails +5v, 0v, and +/-12v. The total off-board loading of these rails should not exceed the ratings in section 2.7.

In addition, an optional power connector, J7, allows Archer to be powered from an off-board supply.

### 5.1 Serial Bus Expansion Header J3

```
                        1    2
                +12V    +    +    -12V
                 +5V    +----+    +5V
                  0V    +----+    0V
Channel A        DCD    +    +    CTS      Channel A
   -     -       RTS    +    +    DTR         -     -
   -     -       TxD    +    +    TxC         -     -
   -     -       RxC    +    +    RxD         -     -
   -     -  RI/Sync     +    +    W/RDY       -     -
Channel B        DCD    +    +    CTS      Channel B
   -     -       RTS    +    +    DTR         -     -
   -     -       TxD    +    +    RxTxC       -     -
   -     -       RxD    +    +    RI/Sync     -     -
   -     -     W/RDY    +    +    CTC-1 output
                        25   26
```

| | | |
|---|---|---|
| DCD | Data Carrier Detect | Inputs |
| CTS | Clear To Send | Inputs |
| RTS | Request To Send | Outputs |
| DTR | Data Terminal Ready | Outputs |
| TxD | Transmit Data | Outputs |
| TxC | Transmit baud Clock | Input |
| RxC | Receive baud Clock | Input |
| RxD | Receive Data | Input |
| RI | Ring Indicator | Inputs |
| W/RDY | Wait/Ready bus synchronisation | Outputs |
| RxTxC | Receive/Transmit common clock | Input |
| CTC-1 | from Counter Timer Circuits | Output |

Note Signal names are the DART manufacturer's, not RS232C names

## 5.2 System Bus Expansion Header J4

```
             1     2
      +12V   +     +    -12V
       +5V   +----+     +5V
        0V   +----+     0V
       A14   +     +    A15
       A12   +     +    A13
       A10   +     +    A11
        A8   +     +    A9
        A6   +     +    A7
        A4   +     +    A5
        A2   +     +    A3
        A0   +     +    A1
        D4   +     +    D7
        D5   +     +    D3
        D2   +     +    D6
        D1   +     +    D0
       /M1   +     +    /INT
    /RESET   +     +    CLK
       /WR   +     +    /MREQ
       /RD   +     +    /IORQ
      /CEX   +     +    IEOX
        0V   +----+     0V
   /BUSACK   +     +    /BUSREQ
     /WAIT   +     +    /NMI
        nc   +     +    VBAT
     /RFSH   +     +    /HALT
            49    50
```

| | | | |
|---|---|---|---|
| A15-A0 | Address lines | * | Output |
| D7-D0 | Data lines | * | Bi-directional |
| /M1 | Z80A signal identifies fetch | | Output |
| /INT | Interrupt signal | | Input |
| /RESET | System reset | | Output |
| CLK | System clock | | Output |
| /WR | Write line | * | Output |
| /MREQ | Indicates address is memory | * | Output |
| /RD | Read line | * | Output |
| /IORQ | Indicates address is I/O | * | Output |
| /CEX | Disables on-board memory | # | Input |
| IEOX | IEO daisy chain extension | # | Output |
| /BUSACK | Acknowledge to /BUSREQ | | Output |
| /BUSREQ | External request for bus control | | Input |
| /WAIT | delays processor for slow I/O | | Input |
| /NMI | non maskable interrupt | | Input |
| /RFSH | Low during a refresh cycle | | Output |
| /HALT | Indicates a processor halt state | | Output |
| VBAT | Battery voltage 3.6V nominal | | Supply |

* These signals go to a high impedance state when a /BUSREQ is issued and granted. They can then be controlled by external hardware. See the Z80A manuals for more details.

# These two lines are Archer expansion signals designed to make system expansion simple, and not standard Z80A signals. Their intended use is detailed below.

### 5.2.1 Memory expansion signal /CEX

The signal /CEX is intended for off-board memory expansion schemes. Normally it is held high or left open circuit, and in this condition the board functions perfectly normally. When taken low however all on-board memory is disabled, but the address and control lines on the bus expansion header are unaffected. It is thus possible for external logic to substitute external memory for the on-board memory. This may be usefull in applications which require abnormally large ammounts of program or data memory.

### 5.2.2 I/O expansion signal IEOX

In the same way that /CEX provides memory expansion, so IEOX provides an expansion signal for the daisy chain interrupt scheme used by Z80A I/O chips. Up to three more devices can be chained onto IEOX, with the whole Archer acting like a single device itself. If more than three additional I/O devices are required, then daisy chain extension schemes such as those in the Z80A manuals can be used.

## 5.3 External Power Input Connector J7

This connector is supplied as an alternative to the mains power supply normally fitted. To save board space J7 is physically located underneath the mains transformer.

| Pin | Signal | Current | Function |
|---|---|---|---|
| 1 | 0V | - | +5V,+/-12V Return |
| 2 | +5V | 700mA | Logic supply |
| 3 | Earth# | - | Protective Earth |
| 4 | +VRaw* | 2mA | Power fail sense |
| 5 | +12V | 50mA | RS232C Drivers +ve |
| 6 | -12V | 50mA | RS232C Drivers -ve |
| 7 | +5V | (700mA) | as pin 2 |
| 8 | 0V | - | as pin 1 |

# The protective earth connection may not be required if the mains supply is of double insulated design.

* The +VRaw signal is used for sensing power failure. If this function is not required, this pin should be tied to +5V or +12V and the potentiometer Rv1 adjusted to give 0V on TP2. When power-fail sensing is required, this pin should be taken to a signal which will fall below a defined voltage at least 10mS before the logic supply (+5V) starts to fall. Rv1 should then be adjusted to trip the comparator IC16c at this voltage. In some cases R21 may need adjusting in value (see circuit diagram at rear).

# 6. INSTALLATION

This section covers basic installation of the mains supply for an Archer single board computer and expansion boards. If you have purchased Archer with the external power connector J7, see section 5.3 above. If you have purchased a cased Archer you need only to refer to the section covering connecting a mains plug.

## 6.1 Mains Wiring

Installing Archer is extremely easy, all you have to do is wire in a fused mains supply in accordance with Figure 6.1. Note that the fuse must be a delay type T0.1A (220-240VAC) or T0.2A (110-120VAC) to ensure appropriate protection.

DO NOT ATTEMPT MAINS WIRING IF YOU ARE NOT QUALIFIED

The whole unit should be mounted inside a case, ensuring that exposed mains conductors (including pcb tracks underneath the solder resist) are at least 3mm away from the case material. If the case is conductive (eg. made of metal) then it must also be protectively earthed to comply with UK safety regulations. Note The minimum clearance distance must be maintained at all times, even if the case can be bowed inwards under pressure. Care should also be taken to ensure that accidental contact to mains conductors cannot be made through vent holes etc.

If you have purchased Archer complete with case and mains cord, you will need to connect a mains plug to the lead supplied.

IMPORTANT

The wires in the mains lead supplied are coloured in accordance with the following international code:

Green-and-yellow : Earth
Blue : Neutral
Brown : Live

THIS APPARATUS MUST BE EARTHED

If the colours of the wires in the mains lead do not correspond with the coloured markings identifying the terminals in your plug, you should proceed as follows:

The wire coloured green-and-yellow must be connected to the terminal marked by the letter E or by the standard safety earth symbol or coloured green or green-and-yellow.

The wire coloured blue must be connected to the terminal marked with the letter N or coloured black.

The wire coloured brown must be connected to the terminal marked with the letter L or coloured red.

### 6.1.1 110V Operation

Although Archer is supplied wired for 220-240V operation, it is a fairly simple matter to adapt the power supply for 110-120V working.

To do this, the link on the component side of the pcb which joins the two primary windings of the mains transformer in series must be removed. It is then possible to wire the two primary windings in parallel using the holes provided. Take care to ensure the correct phasing, see the main circuit diagram for details.

THIS WORK MUST NOT BE ATTEMPTED BY UNQUALIFIED PERSONNEL

### 6.2 Mechanical Mounting

Figure 6.2 shows the Archer pcb mounting hole sizes and positions (holes 'F' and 'P'), note that the four holes 'P' are to accomodate the case support pillars in the Archer case. The fixing centers are designed for mounting Archer, and expansion boards, into a BICC-Vero 'Hi Style' instrument case. This case has been chosen for its good looks, good value for money, simple construction, versatility and ready availability. Also shown are the fixing hole sizes and positions for the two sizes of piggy-back expansion board.

Figure 6.3 gives the cutting details for the serial connector panel on this case. No details of the mains components cut-outs are shown as dimensions vary between manufacturers and also some users may want to put various parts either on the 'front' or the 'rear' panel, depending on the application.

Figure 6.4 shows the recommended outlines of the piggy-back mounted expansion boards. Note that the cut-outs 'P' in the expansion boards are to clear the case support pillars when an Archer case is used.

## APPENDIX A

Table A.1 below contains a summary of the option links and their effects. Where IC pin numbers are shown, they are given counting for a 28 pin device and also counting for a 24 pin device in brackets.

| Link | Affects | signal | Posn 1/in | Posn 2 | Posn 3/out |
|---|---|---|---|---|---|
| Lk1 | IC2 pin 26(24) | Pwr:A13 | A13 | +5v | -- |
| Lk2 | IC3 pin 26(24) | Pwr:A13 | A13 | +5v | -- |
| Lk3 | IC4 pin 26(24) | Pwr:A13 | A13 | +5v | -- |
| Lk4 | IC5 pin 26(24) | Pwr:A13 | A13 | +5v | -- |
| Lk5 | IC2 pin 23(21) | A11:/WR | /WR | A11 | +5v |
| Lk6 | -- no link -- | | | | |
| Lk7 | IC3 pin 28 | Power | 5v | BAT | -- |
| Lk8 | IC3 pin 23(21) | A11:/WR | /WR | A11 | +5v |
| Lk9 | -- no link -- | | | | |
| Lk10 | IC4 pin 28 | Power | +5v | BAT | -- |
| Lk11 | IC4 pin 23(21) | A11:/WR | /WR | A11 | +5v |
| Lk12 | -- no link -- | | | | |
| Lk13 | IC5 pin 28 | Power | +5v | BAT | -- |
| Lk14 | IC5 pin 23(21) | A11:/WR | /WR | A11 | -- |
| Lk15 | -- no link -- | | | | |
| Lk16 | Watchdog | /Reset | Enabled | -- | Disabled |
| Lk17 | Power-down | /NMI | Enabled | -- | Disabled |
| Lk18 | Memory addr | IC2-5 | -------- see figure 3.3 -------- | | |
| Lk19 | PIO-2-A /STB | | 0v | RDY | External |
| Lk20 | PIO-2-B /STB | | 0v | RDY | External |
| Lk21 | PIO-1-A /STB | | 0v | RDY | External |
| Lk22 | PIO-1-B /STB | | 0v | RDY | External |
| Lk23 | RxC-A baud clk | | CTC-1 | CTC-2 | External |

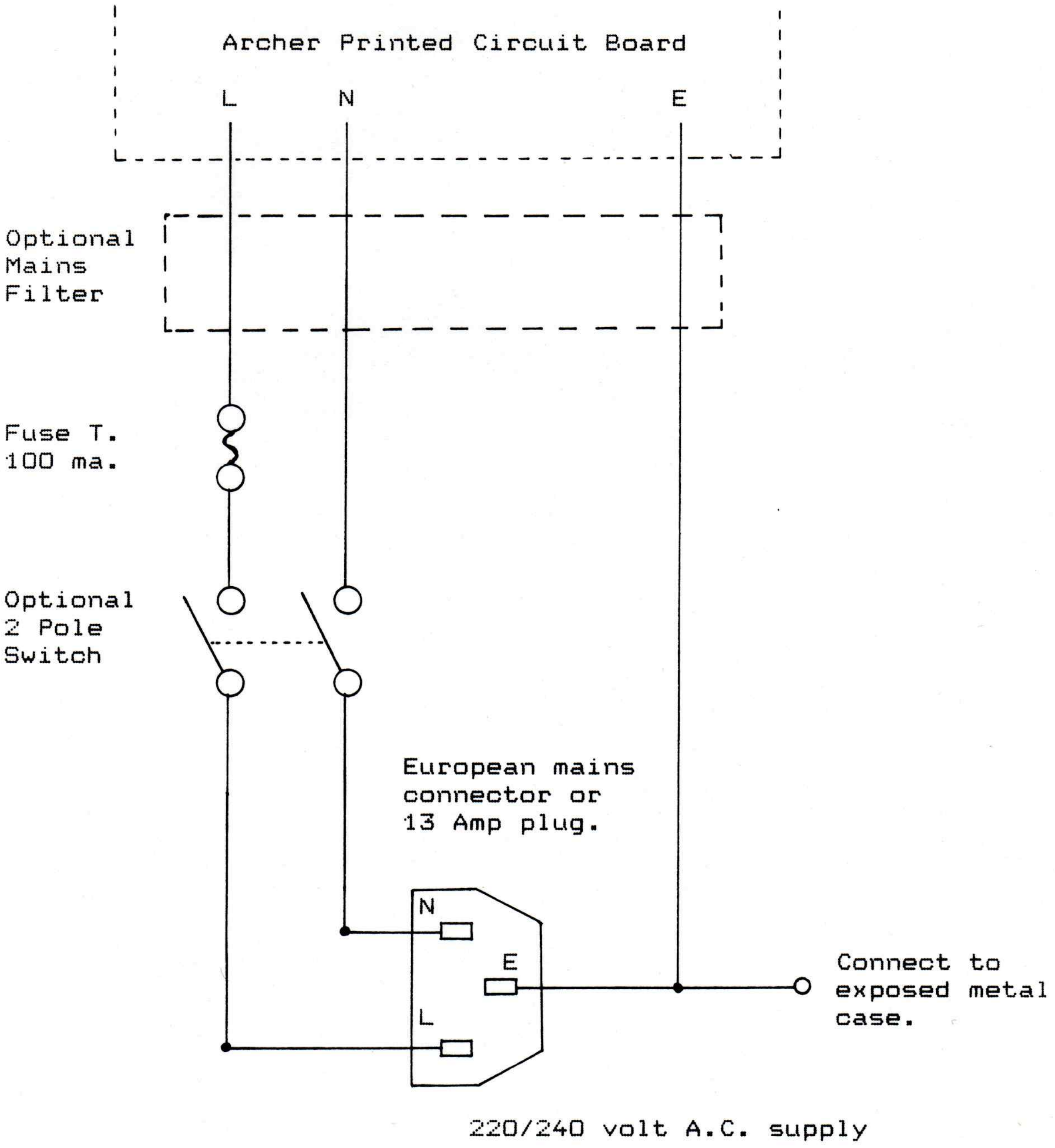
TABLE A.1 Summary of Option links

Table A.2 below lists all of the IO addresses used by Archer, and their functions.

| Address | Device | Function | Section |
|---|---|---|---|
| F0 | CTC and w'dog* | CTC-0 control (SIO-B RxTxC) | 4.1 and 4.4 |
| F1 | | CTC-1 control (SIO-A RxC) | |
| F2 | | CTC-2 control (SIO-A TxC) | |
| F3 | | CTC-3 control | |
| F4 | SIO | SIO-A (J1) data register | 4.2 |
| F5 | | SIO-B (J2) data register | |
| F6 | | SIO-A control register | |
| F7 | | SIO-B control register | |
| F8 | PIO-1 | PIO-1 Port A data | 4.3 |
| F9 | | PIO-1 Port B data | |
| FA | | PIO-1 Port A control | |
| FB | | PIO-1 Port B control | |
| FC | PIO-2 | PIO-2 Port A data | 4.3 |
| FD | | PIO-2 Port B data | |
| FE | | PIO-2 Port A control | |
| FF | | PIO-2 Port B control | |

TABLE A.2 Summary of I/O addreses

* The watchdog hold-off is activated by reads to the address range F0-F3, the same as the CTC status registers.

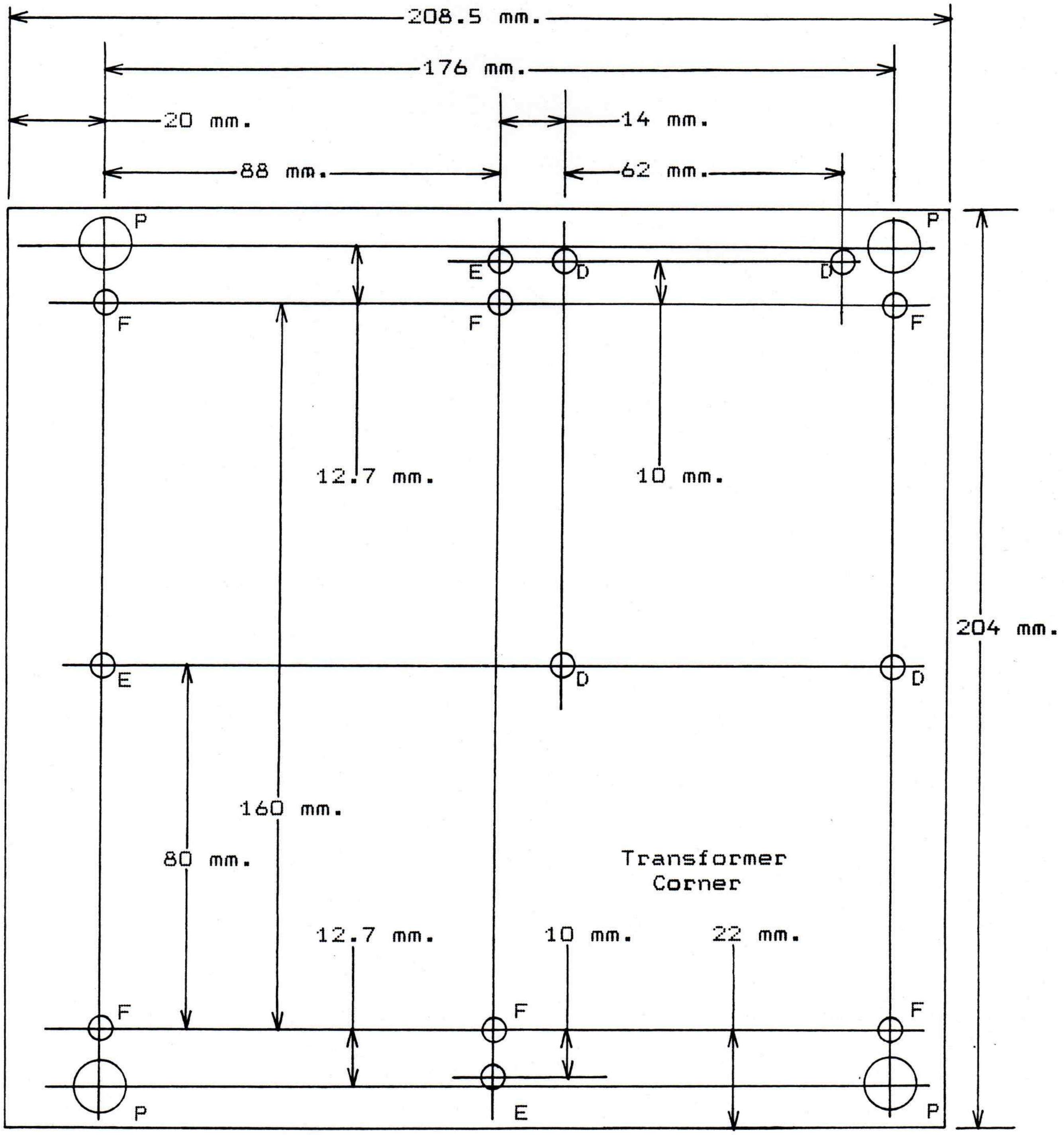

Archer Printed Circuit Board
L
N
E
Optional
Mains
Filter
Fuse T.
100 ma.
Optional
2 Pole
Switch
European mains
connector or
13 Amp plug.
N
E
L
Connect to
exposed metal
case.
220/240 volt A.C. supply

Notes:

1. For 110/120 volt operation, change transformer primaries from series connection to parallel and substitute T. 200 ma. fuse.

2. When using a mains filter, place in it the position shown to protect against transients produced by the on/off switch.

Fig. 6.1. ARCHER MAINS WIRING


208.5 mm.
176 mm.
20 mm.
14 mm.
88 mm.
62 mm.
P
P
E
D
D
F
F
F
12.7 mm.
10 mm.
204 mm.
E
D
D
160 mm.
80 mm.
Transformer
Corner
12.7 mm.
10 mm.
22 mm.
F
F
F
P
E
P

F: 6 fixing holes, 3.7 mm. Dia. Archer main board to case
D: 4 fixing holes, 3.7 mm. Dia. Daughter board 1 to Archer
E: 3 fixing holes, 3.7 mm. Dia. Daughter board 2 to Archer
P: 4 clearance holes, 12 mm. Dia. for case pillars

Fig. 6.2. ARCHER MAIN BOARD DIMENSIONS (component side)

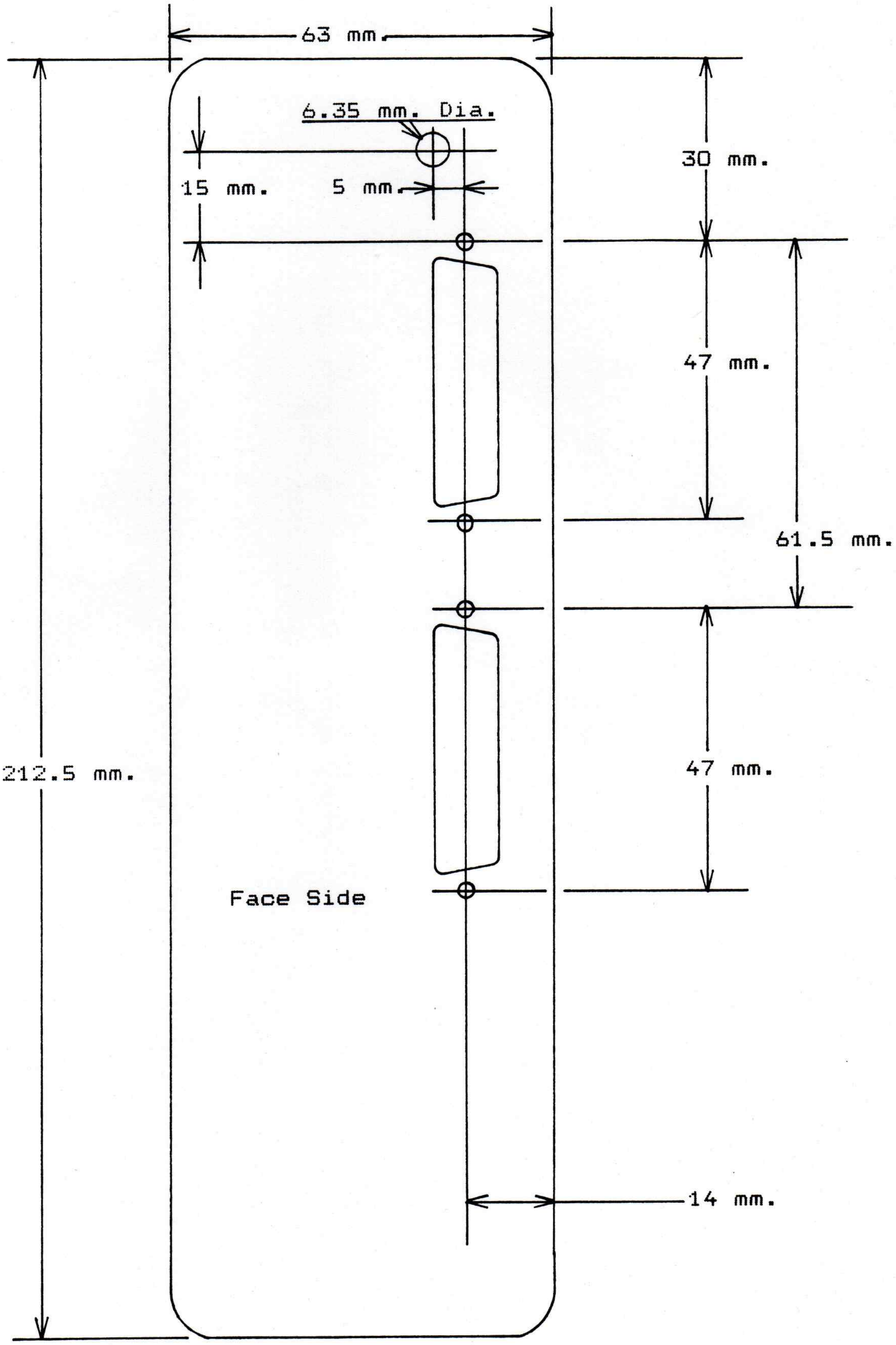
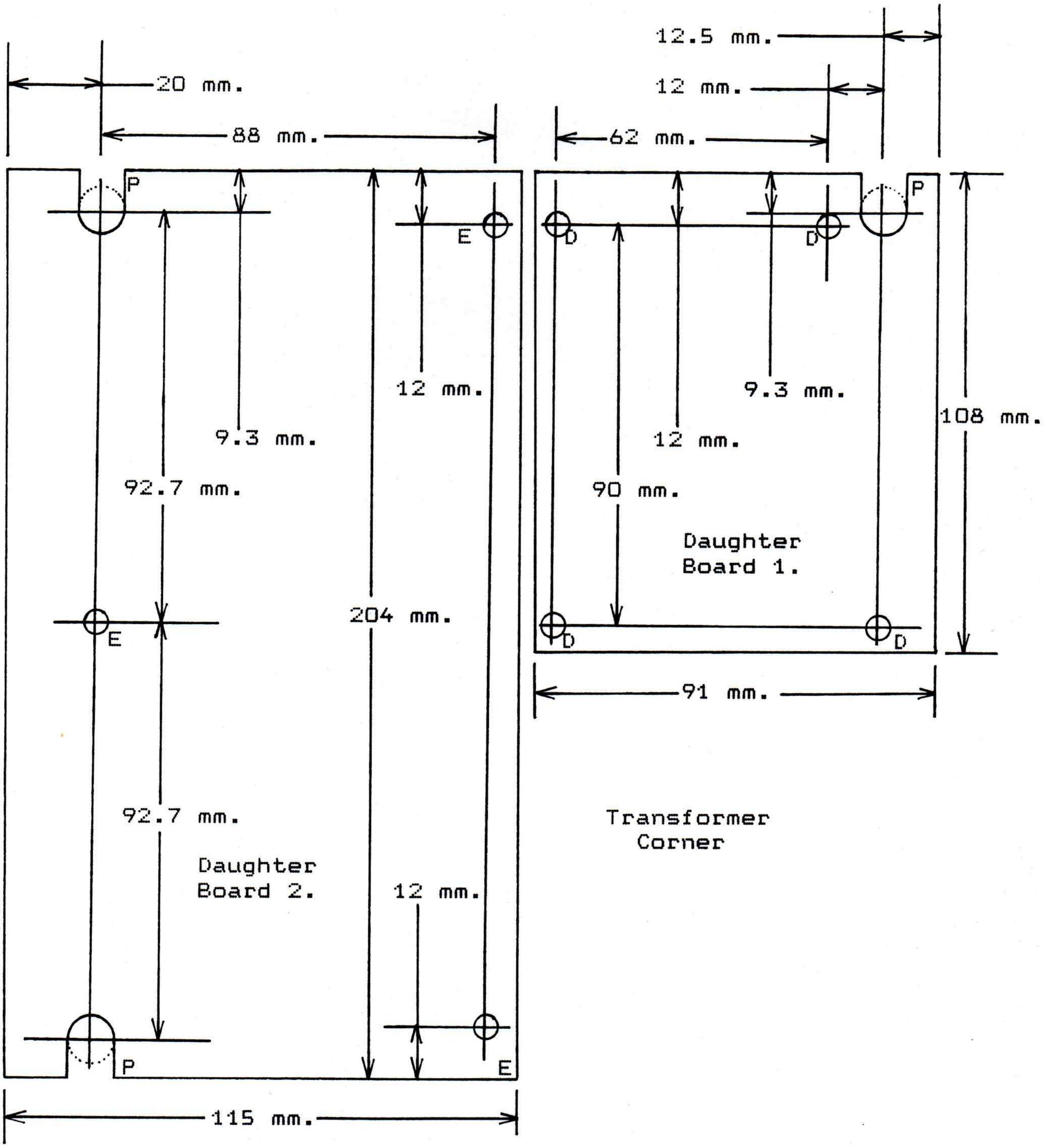
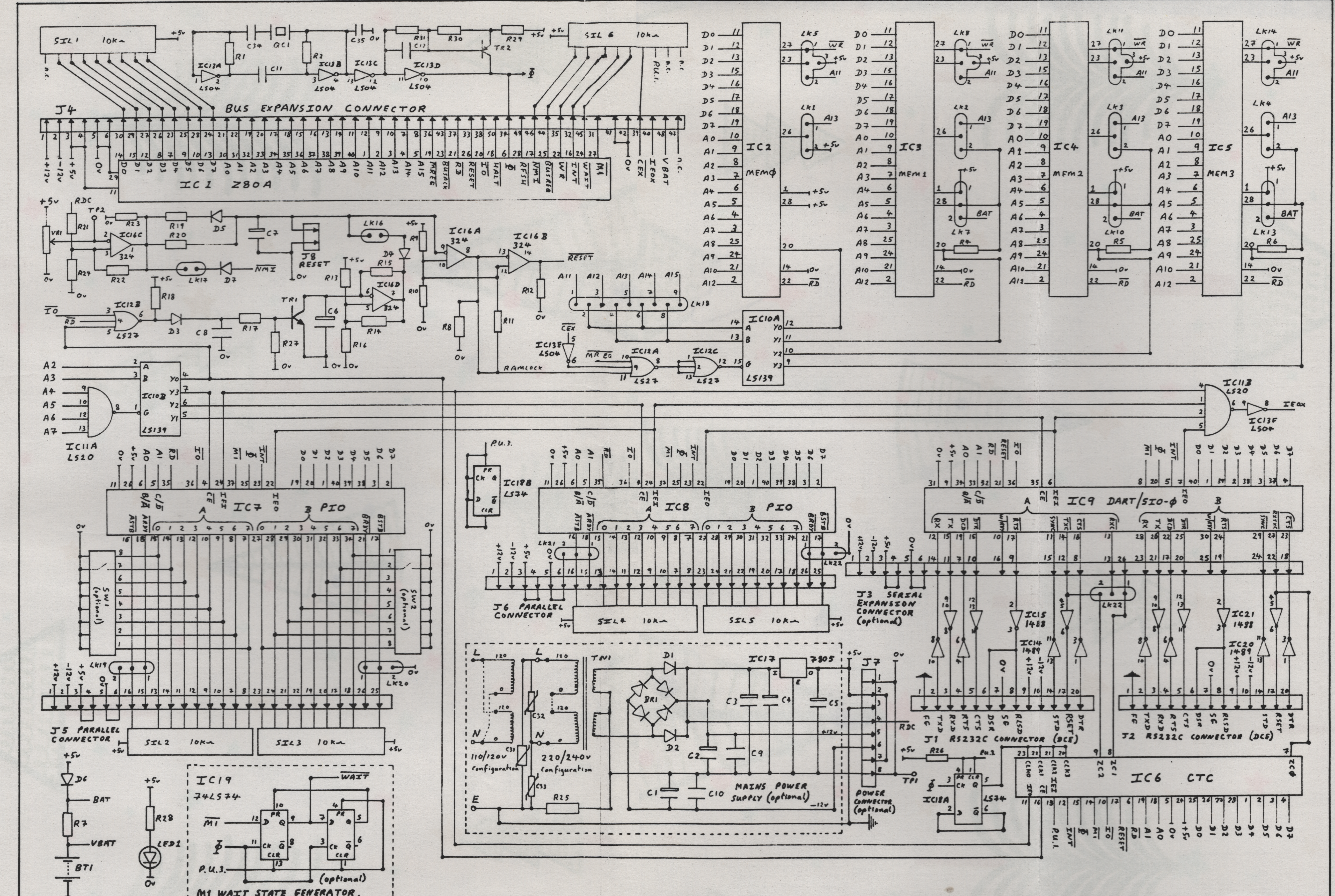

63 mm.
6.35 mm. Dia.
15 mm.
5 mm.
30 mm.
47 mm.
61.5 mm.
47 mm.
212.5 mm.
Face Side
14 mm.

Fig. 6.3. ARCHER FRONT PANEL DIMENSIONS (cased version)


12.5 mm.
20 mm.
12 mm.
88 mm.
62 mm.
P
E
D
D
P
12 mm.
9.3 mm.
9.3 mm.
108 mm.
12 mm.
92.7 mm.
90 mm.
Daughter
Board 1.
E
204 mm.
D
D
91 mm.
92.7 mm.
Transformer
Corner
Daughter
Board 2.
12 mm.
P
E
115 mm.

D: 4 fixing holes, 3.7 mm. Dia. Daughter board 1 to Archer
E: 3 fixing holes, 3.7 mm. Dia. Daughter board 2 to Archer
P: 3 cut-outs based on 12 mm. Dia. holes for case pillars

Fig. 6.4. ARCHER DAUGHTER BOARD DIMENSIONS (component side)


SIL1 10k
SIL 6 10k
BUS EXPANSION CONNECTOR
J4
IC1 Z80A
IC13A LS04
IC13B LS04
IC13C LS04
IC13D LS04
QC1
TR2
IC2 MEMØ
IC3 MEM1
IC4 MEM2
IC5 MEM3
LK5
LK8
LK11
LK14
LK1
LK2
LK3
LK4
LK7
LK10
LK13
IC16A 324
IC16B 324
IC16C 324
IC16D 324
J8 RESET
LK16
LK17
TR1
IC12B LS27
IC12A LS27
IC12C LS27
IC10A LS139
IC10B LS139
IC11A LS20
IC11B LS20
IC13E LS04
IC13F LS04
RAMCLOCK
IEOX
IC7 PIO
IC8 PIO
IC9 DART/SIO-Ø
IC18B LS74
IC18A LS74
J5 PARALLEL CONNECTOR
J6 PARALLEL CONNECTOR
J3 SERIAL EXPANSION CONNECTOR (optional)
SW1 (optional)
SW2 (optional)
SIL2 10k
SIL3 10k
SIL4 10k
SIL5 10k
LK19
LK20
LK21
LK22
IC14 1489
IC15 1488
IC20 1489
IC21 1488
J1 RS232C CONNECTOR (DCE)
J2 RS232C CONNECTOR (DCE)
IC6 CTC
IC17 7805
TN1
BR1
110/120v configuration
220/240v configuration
MAINS POWER SUPPLY (optional)
J7
POWER CONNECTOR (optional)
TP1
TP2
RDC
IC19 74LS74
M1 WAIT STATE GENERATOR.
(optional)
WAIT
P.U.3.
BAT
VBAT
BT1
LED1
D6
R7
R28

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